

ABSTRACT OF THE DISCLOSURE

A 40-Gb/s clock and data recovery (CDR) circuit incorporates a quarter-rate phase detector and a multi-phase voltage controlled oscillator to re-time and de-multiplex a 40-Gb/s input data signal into four 10-Gb/s output data signals. The circuit is fabricated
5 in 0.18 μ m CMOS technology.

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